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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/502,696	02/11/2000	Donald J. Urbas	068856/221	5539

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EXAMINER	
YANG, CLARA I	

ART UNIT	PAPER NUMBER
2635	8

DATE MAILED: 01/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/502,696	URBAS ET AL.	
	Examiner	Art Unit	
	Clara Yang	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 44-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 44-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. This application contains claims 17 - 40 drawn to an invention nonelected with traverse in Paper No. 4. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Response to Arguments

2. Applicant's arguments filed on 15 September 2003 have been fully considered but they are not persuasive.

In response to the Applicant's argument that U.S. Patent No. 5,767,792 (Urbas et al.) fails to teach the limitation of the clock generator no longer supplying current to the memory once the data has been read from memory as called for by claims 1 and 13 (see pages 13 and 14) or when the data has been read into memory as called for by claim 7 (see pages 13 - 14), Urbas teaches a transponder having a READ mode, wherein data is read from EEPROM 25, and a PROGRAM mode, wherein data is written into EEPROM 25 (see Col. 6, lines 61 - 67; Col. 7; Col. 8, lines 1 - 10; Col. 12, lines 1 - 67; Cols. 13 - 14; and Col. 15, lines 1 - 21).

Per Urbas, during the READ mode, the OUTPUT ENABLE signal produced by data sequence generator 26 goes high in order for EEPROM 25 to output data onto data bus 30 and goes low in order to tri-state EEPROM 25's output (see Col. 7, lines 57 - 60). It is understood that when the OUTPUT ENABLE signal goes high, a current flows from data sequence generator 26 to EEPROM 25, whereas when the OUTPUT ENABLE signal goes low, no current flows from data sequence generator 26 to EEPROM 25. Consequently, Urbas does teach the limitation of ceasing the supply of current to a memory once its data has been output to a data module.

During the PROGRAM mode, Urbas imparts that address and timing generator 23 generates a WRITE ENABLE signal to programming timing generator 80, both of which are understood to form a clock generator, and that the write cycle begins with programming timing generator 80 outputting a high EHV1 signal for 5.63 ms in order to erase the data in the byte being addressed (see Col. 14, lines 33 - 42). In other words, programming timing generator 80 supplies a current (EHV1) to EEPROM 25 for erasing data. For the next 176 μs, EHV1 and EHV2 are low (i.e., no current is supplied to EEPROM 25). Then for the next 5.63 ms, EHV1 remains low and EHV2 is high in order to write the data in the addressed byte (see Col. 14, lines 45 - 51.) Here it is understood that once the data has been written to EEPROM 25, EHV1 and EHV2 remain low until the next writing cycle. In other words, no current is provided from programming timing generator 80 to EEPROM 25 after data has been read into EEPROM 25. Consequently, Urbas does teach the limitation of ceasing the supply of current to a memory once data has been read into memory.

3. In response to applicant's argument on page 15 and 17 that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Regarding U.S. Patent No. 5,517,194 (Carroll et al.), Carroll, like Urbas, teaches a passive transponder that can read selected data from or write selected data to its non-volatile memory (see Carroll, Col. 2, lines 27 - 30 and 60 - 67 and Col. 3, lines 1 - 6). However, in addition to

having a read mode and a write mode, Carroll's passive transponder has four lock bits (bits 12, 13 ,14, and 15) contained to word 0 (i.e., "status byte") of the non-volatile memory 48 (see Col. 17, lines 32 - 38). Carroll teaches that if bit 15 of word 0 (which corresponds to lock bit L0 in Fig. 4A) is logic 1, then all 16 rows (i.e., rows 0 - 15) of the memory are locked (see Col. 15, lines 25 - 29). If bit 14 of word 0 is (which corresponds to lock bit L1 in Fig. 4A) is logic 1, then only the status byte (i.e. word 0) is locked (see Col. 15, lines 44 - 46). Because Carroll teaches that a lock bit of word 0 cannot be changed once it is set (see Col. 17, lines 22 - 23), it is understood that bits 4 and 15 are seal bits. Carroll also imparts that various areas of memory 48 can be locked by setting bits 12 and 13. For example, if bit 12 (which corresponds to L3 in Fig. 4A) is logic 1 while bit 13 is logic 0, rows 1 - 5 of memory 48 are locked. If bit 12 is logic 0 while bit 12 while bit 13 is logic 1, then rows 1 - 3 of memory 48 are locked. If bits 12 and 13 are both logic 1, then rows 1 - 7 of memory 48 are locked. (See Col. 15, lines 37 - 44.) Here it is understood that bits 12 and 13 of the status byte are mode bits. Urbas' status byte, on the other hand, has only one bit that is set to logic 1 to lock the entire contents of a memory device.

Regarding Young (U.S. Patent No. 5,978,192), Young teaches a protection circuit that is effective for protecting integrated circuits against a DC over-voltage condition. Urbas' transponder is formed as an integrated circuit (see Col. 16, lines 40 - 46 and 52 - 57). Urbas teaches that detector 21 includes the necessary over-voltage protection for proper operation of the transponder (see Col. 4, lines 46 - 48). Because clamps limit the peak voltage of a semiconductor device and detector 21 is housed in chip 710, which is a semiconductor device, it is understood that detector 21 includes a semiconductor clamp to provide over-voltage protection.

Specification

4. The abstract of the disclosure is objected to because the maximum word limit of 150 words has been exceeded. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 4, 6 – 8, 10, 11, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipate by U.S. Patent No. 5,767,792 (Urbas et al.).

Referring to Claims 1, 7, and 13, as shown in Fig. 1, Urbas' transponder comprises (a) an EEPROM 25 with 16 addressable bytes for storing data (see Col. 1, lines 51 – 52 and 61 – 65; and Col. 7, lines 53 - 54). Because sequence generator 26 uses the 8th data bit of the 16th byte to determine whether or not to allow mode decoder 27 to look for a command sequence that places the transponder in the program mode (see Col. 6, lines 7 – 13), it is understood that the 16th byte is a status byte region and that the remaining 15 bytes form the data region of EEPROM 25. Urbas' transponder also includes: (b) an address and timing generator 23 for outputting an OUTPUT ENABLE (or read) signal via data sequence generator 26 and a WRITE ENABLE (or program) signal to programming timing generator 80, wherein both signals supply current to EEPROM 25 (see Col. 7, lines 54 – 64 and Col. 14, lines 8 - 51); (c) a divider 70*b* (see Fig. 2) or address module for addressing an address in EEPROM 25 in response to a clock signal from address and timing generator 23 (see Col. 4, lines 59 – 67 and Col. 5, lines 1 – 11); (d) a data bus 30 and a universal shift register 11 for receiving the data stored in EEPROM 25 at an

address indicated by address and timing generator 23 and for inputting data into EEPROM 25 (see Col. 7, lines 63 - 65; Col. 8, lines 1 - 10; and Col. 14, lines 1 - 12); and (e) data sequence generator 26 and mode decoder 27 for reading the status byte and outputting a program enable signal in response to the 8th data bit (see Col. 6, lines 7 - 13). Here it is understood that: (1) divider 70*a* of address and timing generator 23 (see Fig. 2), data sequence generator 26, and programming timing generator 80 form a clock generator; (2) data bus 30 and universal shift register 11 form a data module; and (3) data sequence generator 26 and mode decoder 27 form a program control. During the READ mode, Urbas teaches that data sequence generator 26's low OUTPUT ENABLE signal (i.e. no current supply) tri-states the output of EEPROM 25 once its data has been output to the data module as to avoid conflicting with data from buffer 9 and multiplexer 9A (see Col. 7, lines 57 - 60). According to Urbas, in order to place transponder 100 in the PROGRAM mode, address and timing generator 23 receives a program signal from mode decoder 27 and outputs a data latch signal (or WRITE ENABLE signal) that causes programming timing generator 80 to start the write cycle and to have the data in shift register 11 written to EEPROM 25 (see Col. 6, lines 31 - 44).

Regarding Claim 2, Urbas teaches that the A_0-A_3 outputs (or address clock signal) of divider 70*b* are used to sequentially address the bytes of EEPROM 25 via address bus 28 (see Col. 5, lines 3 - 6). Here it is understood that each address clock signal is increased sequentially by divider 70*b* in order to change the address of EEPROM 25 as identified by address and timing generator 23. Address and timing generator 23 also sends a signal to data sequence generator 26 (see Fig. 1) that causes data sequence generator 26 to produce a high OUPUT ENABLE signal to EEPROM 25, thus permitting EEPROM 25 to output its data (see Col. 7, lines

53 - 67). Here it is understood that a high OUTPUT ENABLE signal provides a supply current to EEPROM 25.

Regarding Claim 3, as shown in Fig. 1, Urbas' clock generator outputs (a) a WRITE ENABLE signal or program signal that supplies current to EEPROM 25 in order to program EEPROM 25 (see Col. 14, lines 8 - 12 and 33 - 51); and (b) an address clock signal or latch signal (see Col. 4, lines 59 - 64). In response to the address latch signal the clock generator, divider 70*b* (or address module) selects a specific address of EEPROM 25 (see Fig. 2, divider 70*b*, outputs A_0-A_3; and Col. 5, lines 3 - 8). The data module inputs data into memory at the address indicated by the address module (see Col. 13, lines 61 - 67 and Col. 14, lines 1 - 12). Once the data in the data module has been stored in memory, the clock generator stops sending the WRITE ENABLE signal, thus turning off EEPROM 25 and allowing the transponder to resume transmission of the RECEIVE CLOCK signal to the interrogator (see Col. 14, lines 52 - 59).

Regarding Claims 4 and 8, Urbas' transponder has an EEPROM 25 with 16 addressable bytes (see Col. 7, lines 53 - 56). As explained above in Claim 13, it is understood that the 16th byte is a status byte region and that the remaining 15 bytes form the data region of EEPROM 25 and that data sequence generator 26 and mode decoder 27 form a program control. Urbas discloses that once the transponder is in the program mode, the clock generator outputs the WRITE ENABLE signal to the programming timing generator 80, thus starting the write cycle and causing the data received from the interrogator to be written to EEPROM 25 at the desired address (see Col. 6, lines 31 - 44).

Regarding Claims 6 and 10, Urbas imparts that the if the 8th data bit of EEPROM 25's 16th byte is set to logic 1 and that the transponder's power level is adequate for programming, the transponder enters the programming mode and writes the data on data bus 30 to the desired

address of EEPROM 25. If the 8th data bit of EEPROM 25's 16th byte is cleared or set to logic 0, the transponder is prevented from entering the programming mode. (See Col. 6, lines 7 - 13 and 31 - 49.) Here it is understood that the 8th data bit of EEPROM 25's 16th byte is an HLOCK bit.

Regarding Claim 11, Urbas teaches that when a transponder receives sufficient power from an interrogator, the transponder enters the program mode after receiving three predetermined pulses from the interrogator (see Col. 12, lines 42 - 53). Because the three pulses must be received by the transponder within a predetermined time window (i.e. during the transmission of EEPROM 25's 16th byte of data), it is understood that the three pulses are pulse space modulated. Furthermore, because Urbas expresses that a user can specify any address of EEPROM 25 to be written to (see Col. 15, lines 1 - 12) and that the master clock is disabled during the write cycle to prevent the clock generator for selecting the next address (see Col. 14, lines 42 - 45), it is implied that the clock generator supplies an address latch signal once an interrogator transmits three pulses to change the transponder's operation mode from read to program, a first byte of data, and a 9th bit indicating that the data is to be written to that specific address.

Regarding Claim 15, Urbas imparts that the if the 8th data bit of EEPROM 25's 16th byte is set to logic 1 and that the transponder's power level is adequate for programming, the transponder enters the programming mode and writes the data on data bus 30 to the desired address of EEPROM 25. If the 8th data bit of EEPROM 25's 16th byte is cleared or set to a logic 0, the transponder is prevented from entering the programming mode. (See Col. 6, lines 7 - 13 and 31 - 49.) Here it is understood that the 8th data bit of EEPROM 25's 16th byte is an HLOCK bit.

Referring to Claim 16, Urbas' transponder has means for generating a preamble to indicate the voltage level of signal received from the interrogator and transmitting the preamble to the interrogator. As shown in Fig. 1, the transponder has a detector 21 that provides direct current (DC) power to the transponder and detects a received signal's envelope, which is used to establish the PROG DATA signal (see Col. 4, lines 40 - 48). Because Urbas teaches that PROG DATA is low (or "0") when the supply voltage is less than three volts and high (or "1") when the supply voltage is greater than 3 volts (see Col. 8, lines 59 - 61), it is implied that detector 21 has a comparator. Urbas illustrates in Fig. 8 the transponder's preamble generator. If the transponder's supply voltage is greater than 3 volts, the preamble starts high and goes low (i.e., the first voltage indicator signal indicating PROG DATA's logic level of "1"). If the transponder's supply voltage is less than 3 volts, the preamble starts low and goes high (i.e., the second voltage indicator signal indicating PROG DATA's logic level of "0"). (See Col. 8, lines 39 - 67.)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 5, 9, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,767,792 (Urbas et al.) as applied to claim 1 above, and further in view of U.S. Patent No. 5,517,194 (Carroll et al).

Regarding Claims 5, 9, 12, and 14, the status byte of Urbas' transponder lacks two seal bits that enables the transponder to be programmed if at least one of the seal bits is clear (i.e., logic "0") and a mode bit that prevents the address module from accessing the addresses in memory not corresponding to the mode indicated by the mode bit.

In an analogous art, Carroll's passive transponder has four lock bits contained to word 0 of the non-volatile memory 48 (see Col. 17, lines 32 - 38). Carroll teaches that if bit 15 of word 0 (which corresponds to lock bit L0 in Fig. 4A) is logic 1, then all 16 rows (i.e., rows 0 - 15) of the memory are locked (see Col. 15, lines 25 - 29). If bit 14 of word 0 is (which corresponds to lock bit L1 in Fig. 4A) is logic 1, then only the status byte (i.e. word 0) is locked (see Col. 15, lines 44 - 46). Because Carroll teaches that a lock bit of word 0 cannot be changed once it is set (see Col. 17, lines 22 - 23), it is understood that bits 4 and 15 are seal bits. Carroll also imparts that various areas of memory 48 can be locked by setting bits 12 and 13. For example, if bit 12 (which corresponds to L3 in Fig. 4A) is logic 1 while bit 13 is logic 0, rows 1 - 5 of memory 48 are locked. If bit 12 is logic 0 while bit 12 while bit 13 is logic 1, then rows 1 - 3 of memory 48 are locked. If bits 12 and 13 are both logic 1, then rows 1 - 7 of memory 48 are locked. (See Col. 15, lines 37 - 44.) Here it is understood that bits 12 and 13 of the status byte are mode bits.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the status byte of Urbas' transponder as taught by Carroll,

because a status byte with seal bits and mode bits provides a user with better means for managing a memory device than a status byte with only one bit that is set to logic 1 to lock the entire contents of a memory device.

10. Claims 44 - 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,767,792 (Urbas et al.) as applied to claim 1 above, and further in view of U.S. Patent No. 5,978,192 (Young et al.).

Regarding Claims 44 - 47, because Urbas discloses that passive transponder 100 in Fig. 9 – 12 includes a substrate 700 and a chip 710 that houses each of the transponder's structures including EEPROM 25, it is implied that Urbas' transponder is formed as an integrated circuit (see Col. 16, lines 40 – 46 and 52 – 57). Urbas teaches that detector 21 includes the necessary over-voltage protection for proper operation of the transponder (see Col. 4, lines 46 – 48). Because clamps limit the peak voltage of a semiconductor device and detector 21 is housed in chip 710, which is a semiconductor device, it is understood that detector 21 includes a semiconductor clamp to provide over-voltage protection. Urbas, though, is silent that the clamp is formed by a complementary metal-oxide semiconductor (CMOS) circuit.

In an analogous art, Young teaches that clamp can be configured as a CMOS integrated circuit (see Figs. 3 and 4) or a bipolar integrated circuit (see Col. 1, lines 23 – 25). The clamp circuit in Fig. 4 has a CMOS inverter circuit 60 that comprises of an N-MOSFET 70 and a P-MOSFET 80.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the clamp of Urbas' transponder as taught by Young, because a CMOS integrated clamp circuit uses very little power.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clara Yang whose telephone number is (703) 305-4086. The examiner can normally be reached on 8:30 AM - 7:00 PM, Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (703) 305-4704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

CY
29 December 2003

BRIAN ZIMMERMAN
PRIMARY EXAMINER